UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/301,284	04/28/1999	SHUICHI TAKAYAMA	NAK1-BG86	5392

7590 01/15/2003

Joseph W. Price, Esq.
SNELL & WILMER LLP
1920 Main Street
Suite 1200
Irvine, CA 92614-7060

EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	20

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/301,284	TAKAYAMA ET AL.	
	Examin r	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11, 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the communication filed on 10/28/2002.

Claim 49 is added. Claims 1, 10 are amended. Claims 1-11, and 49 are pending in the application.

Specification objection

2. The amended claim 1 and newly added claim 49 recite, ***"the position of which does not correspond to a byte boundary".*** With regard to this limitation, the specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. With regard to the new added limitation in claim 49, ***"cycling though m different values, with m is not being a power of two",*** the specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Both newly added limitation ***"of which does not correspond to a byte boundary"*** and ***"cycling though m different values, with m is not being a power of two"*** is negative limitations. The specification does not describe the limitations as being claimed. The coverage of negative limitations causes to introduce new subject matter. Thus, it makes the specification fail to provide a proper antecedent basis for ***"the position of which does not correspond to a byte boundary",*** and ***"cycling though m different values, with m is not being a power of two"***. Therefore, the specification is objected to. To overcome the objection, the claim-amended limitation must be described in exact term so that it is disclosed in the in the specification. For example, take m = 25, which is not a power of 2; then the teaching of this feature, is not disclosed in the specification.

In the specification, it discloses a 32-bit address used for describing program counters (spec: pages 35-36), where the lower 3-bit is used to specify an instruction unit included in the instruction packet. This corresponds to the claim limitation: **a position of processing target instruction** in describing the **second program counter**. The description of the second program counter in this spec does not cover or

nearly connect the limitations "***of which does not c rrespond to a byte boundary***" and "**m is n t a power of 2**" as claiming.

Response to Arguments

3. Applicant's request for reconsideration and arguments have been fully considered but they are not persuasive.

-Regarding the amended claim 10, the prior rejection under 35 U.S.C. 112, second paragraph applied to claims 10-11 is withdrawn.

-Regarding the applicant's argument that Christie's program counter (less significant program counter) does not anticipate the claimed limitation "**the position of which does not correspond to a byte boundary**".

- Examiner respectfully disagrees: A counter is known in the art. A program counter is also known in the art for pointing a position of an instruction. As previously claimed by applicant (first amendment) "*the second program counter indicating a position of processing target instruction in the processing packet* ***regardless*** *of whether the position corresponds to a byte boundary,* and now amendment, "of which does not correspond to a byte boundary", this is clearly to the examiner that the new claim limitation is inconsistent to the specification. The new amended limitation also contradicts to the limitation "*the second program counter indicating a position of processing target instruction in the processing packet*". Moreover, claiming for 'not a byte boundary' is negative limitation. Applicant is respectful asked to review MPEP for this subject matter (also: Schechter, 205 F.2d 185, 98 USPQ 144 (CCPA 1953)).

By further reviewing the specification, the spec describes the second counter as a 3-bit counter. The value in the counter is 001, 010, 100, and might be the value of other combination of the 3 bits. As a result, its value varies from 000 to 111 made by 8 different combinations. For example, in the spec, it wrote, "001 points to the first unit in an instruction packet" (page 36).

Regard to the Christie counter, it is 4-bit counter. In the same manner of the specification, Christies takes the least significant 4 bits in a 32-bit counter to form the second counter. The values in Christies' counter

might be ranged from 0000 to 1111. However, it takes only four decodes for pointing 4 ROP instructions. Therefore, it has the similar functionality to the description of the second counter described by the spec pages 35-36 because both the second counter in claim and Christies' are point to an instruction. Claimed invention's second counter points to an instruction within the packet (spec page 36); Christies' counter points to an instruction between 4 ROPs. Either the argument or the recited limitation "does not correspond to a byte boundary" does not make the counting function different, and thus cannot be persuasive.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11, 49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The new limitations *"of which does not correspond to a byte boundary"* as amended in claim 1, and *"m is not being a power of 2"* as amended in claim 49, fail for being supported by the specification. The limitations which are not supported by the invention, or fail to disclose within the scope of specification for making and using it, in such full, clear, concise, and exact terms would not be enable any person skilled in the art to pertain. The limitations *"of which does not correspond to a byte boundary"*, and *"m is not being a power of 2"* are negative limitations that draw no boundary for what it is excluded. 'm' is an arbitrary number. Therefore, if it would be a large number, no technology at the time of the invention would be enabled without undue experimentation.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11, 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1-11:

Claim 1 recites, "*the position of which does not correspond to a byte boundary*". This limitation is indefinite because the meaning of "a byte boundary" is unclear. Since the specification describes a value in the second counter which might be 001, 010, 100, or a value which is not limited to one of these values. This indicates that the counter consists all values formed by the combination of 3 bits. A position of the processing target instruction might vary from 000 to 111. It is not clear whether one of these values is a byte boundary or no value in 000 to 111 is a "byte boundary".

The newly added limitation, "*the position of which does not correspond to a byte boundary*" is negative limitation. Negative limitation renders the claim indefinite because it's an attempt to claim the invention by excluding what the inventors did not invent rather than distinctly and particularly pointing out what they did invent (Schechter, 205 F.2d 185, 98 USPQ 144 (CCPA 1953)).

The indefinite limitation, which is identified in the claim 1, renders the scope of claims 1-11 indefinite. Therefore the claims 1-11 are rejected under the quotation of the second paragraph of 35 U.S.C. 112.

As per claim 49: The claim 49 also recites, "the position of which does not correspond to a byte boundary". The rejection of the claim 49 upon this limitation is corresponding to the reason as set forth in the claim 1. The claim 49 further recites, "*cycling though m different values, with m is not being a power of two*". This limitation is also indefinite because it is the negative limitation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Christie et al., US Patent No. 5,559,975.

As per claim 1:

-Regarding claim limitations:

"*A processor for reading instructions from a memory according to a program counter, and for executing the read instructions,*

the program counter including a first program counter and a second program counter,

the first program counter indicating a storage position of a processing packet in the memory, the processing packet being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary "

Christie's reference teaches the claim limitations by using (4:31) bits (*first program counter*), named as more significant program counter, to position to a byte boundary of a RISC instruction set or a X86 instruction. The counter increments or branches to the next instruction set of RISC or X86 using a multiplexer 761 (see column 18, lines 24-38).

-Regarding claim limitations:

"*the second program counter indicating a position of processing target instruction in the processing packet, the processing target instruction being an operation to be executed by the processor, and the position of which does not correspond to a byte boundary* ",

Christie's reference teaches the claim limitations by using a set bit (0:3) (*second program counter*) which is decoded to run through the 4 bits of a ROP (see column 18, lines 9-10), where the decoder counter

which points to a ROP would be a set four values, each value indicates a position of a target instruction within a ROP instruction set.

As per claim 2:

-Regarding claim limitations of claim 2, Christie teaches further claim limitations "first program counter updating and second program counter updating" using the incrementer, adders, and multiplexers (see column 18, lines 4-23, and lines 24-38).

As per claim 3:

-Regarding claim limitations of claim 3, claim 3 is inherent from relative address values used in a program when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38) to perform adding that sets the address of the relative address value in the program counters. To perform the adding a relative value included in an instruction, Christie discloses that in a branch, an instruction is fetched and decoded. The counter identifies the next address of the target instruction, and uses adders, selectors, to form the next address (this mechanism is provided in the discussion column 18, lines 4-38).

As per claim 4:

-Regarding claim limitations of claim 4, claim 4 manipulates a calculation performed by adders in the first counter in the second counter. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 5:

-Regarding claim limitations of claim 5, claim 5 manipulates a calculation performed by adders in the first counter in the second counter corresponding to the functionality of claim 4. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 6:

-Regarding claim limitations of claim 6, claim 6 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 7:

-Regarding claim limitations of claim 7, claim 7 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 8:

-Regarding claim limitations of claim 8, claim 8 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 9:

-Regarding claim limitations of claim 9, claim 9 is inherent from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 10:

-Regarding claim limitations of claim 10, given the broadest interpretation of the claim in light of specification, Christie's processing packet is ROP which has a length number 4. Christie discloses the program counter (4:30) that is more significant than 4, the length of ROP.

As per claim 11:

-Regarding claim limitations of claim 11, functionality claim 11 is inherent in registers, read/write address buffers, cache, and fetch mechanism used to store data as shown in Christie's figures (Figures 1A...).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Christie et al., US Patent No. 5,559,975.

As per claim 49:

-Regarding claim limitations of claim 49, functionality claim 49 is corresponding to the functionality of claim 1. Claim 49 further recites "*the second counter indicating a position of possessing target instruction in the processing packet, by cycling through m different values, with m not being a power of 2*". Christies discloses a second counter decoder which points to 4 instructions of a ROP. The 4 is a power of 2. However, Christies suggests about super scalar CISC in which its instruction's formation is known as sets of complex instructions. A complex instruction set has a set of instructions which is not power of 2. Therefore, it would be obvious to an ordinary skill in the art when performing counting of an instructions set in which the length of the set is not power of 2, would modify the counter to go through the length of that number. Doing so would correspond to the number of instructions required for counting.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be

reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Morse, can be reached on (703) 308-4789.

The fax phone numbers for this Group are:

Official: (703) 746-7239.

After Final: (703) 746-7238.

Non-Official: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TTV
January 9, 2003

GREGORY MORSE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100